ABSTRACT

A method to reduce the inverse narrow width effect in NMOS transistors is described. An oxide liner is deposited in a shallow trench that is formed to isolate active areas in a substrate. A photoresist plug is formed in the shallow trench and is recessed below the top of the substrate to expose the top portion of the oxide liner. An angled indium implant through the oxide liner into the substrate is then performed. The plug is removed and an insulator is deposited to fill the trenches. After planarization and wet etch steps, formation of a gate dielectric layer and a patterned gate layer, the NMOS transistor exhibits an improved Vt roll-off of 40 to 45 mVolts for both long and short channels. The improvement is achieved with no degradation in junction or isolation performance. The indium implant dose and angle may be varied to provide flexibility to the process.